The CDF Run II Silicon Detector

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Abstract

The 8 layer, 750k channel CDF Run II silicon detector is an essential part of the heavy flavor tagging and forward tracking capabilities of the CDF experiment. A summary of the experience in commissioning and operating this double-sided silicon micro-strip detector during the first three years of Run II is given. The challenges associated with running a silicon detector as part of the L2 trigger are described. Results from off-line reconstruction showing the detector resolution, efficiency, and aging as well as the impact of the silicon detector on physics program of the experiment are presented.

Summary

While the Run II upgrades for increased luminosity and higher center-of-mass energies ($\sqrt{s}$) at Fermilab's Tevatron were being completed, The Collider Detector at Fermilab (CDF) replaced the Run I silicon tracker with an entirely new detector; the Silicon Vertex Detector II (SVXII). The SVXII has nearly twice the coverage of both the luminous region and pseudo-rapidity (η) of its Run I predecessor with the ability to do three dimensional tracking and more precise impact parameter resolution for better B-tagging. SVXII is one of three silicon sub-detectors which also include Layer Zero Zero (L00) and the Intermediate Silicon Layers (ISL) which together provide up to 8 layers of coverage with 722,432 total channels. The inner-most sub-detector, L00, is a radiation hardened, single-sided, layer of 48 ladders mounted directly to the beam pipe, 1.5cm from the beam line. SVXII consists of 6 axial "barrels" divided into 12 ϕ-slices each with 5 radial, double-sided, layers between 2.5 and 10.6 cm. The ISL is composed of 296, double-sided, ladders between 20 and 28 cm and covers the area between SVXII and the CDF wire tracker (COT). The ISL is 1.9m long and provides silicon hits out to $|\eta| < 2$.

The three sub-detectors share the same basic readout system, starting with the custom SVX3D chip, an ASIC with 128 channels and a 46 capacitor analog storage pipeline allowing for "deadtimeless" data acquisition *i.e.* charge is integrated on one capacitor while data is read out on another. The SVX3D also features common mode noise suppression, sparsification, and other settings used to optimize the charge collection. A "wedge", of up to 5 ladders, is serviced by one "portcard" mounted near the detector. The portcard serves as a switch-yard, bringing analog, and digital voltages, and electrical control signals to the chips and bias voltages to the attached silicon. The portcard also converts the outgoing data from electrical to optical for transmission to the VME-based data acquisition system which controls the entire detector and presents data to the Level 2 and Level 3 trigger systems. L00, SVXII, and the ISL are all incorporated in the same power distribution, cooling, interlock, and radiation protection systems.

Commissioning began early 2001 and the Run II detector steadily progressed towards a robust operating point but was significantly hampered by problems from which lessons for future detectors should be drawn. Setbacks in commissioning included:

- Complications in detector installation enhanced by the late delivery of power supplies. The late schedule led to incomplete testing and debugging of the the interlock mechanisms which later put the detector at risk.
- A lack of testing under realistic conditions which led most notably, to the installation of

the ISL with an undetected blockage in the cooling lines that later required boring with a laser.

- Excess noise in L00 leading to common mode pedestal fluctuations which cannot be suppressed off-line.
- Optical power mismatches between data transmitters and receivers.
- Loss of wirebonds due to Lorentz forces as synchronous trigger conditions resonate Aluminum wirebonds causing fatigue and eventual failure.

Failure modes that appeared during commissioning have largely been understood and procedures have been implemented to avoid further damage. In spite of the unforeseen challenges, the system is currently running stably with over 92% of the system operational and more than 84% producing quality data.

Sensors in the detector are operated with signal to noise ratios of between 11 and 15 depending on the ladder type. With high signal to noise, single hit efficiencies can be kept at greater than 99% without producing prohibitive data volume. Tracking resolution continues to improve as the global and relative alignment is better understood by looking at tracks in data. In addition, cluster resolution meets specifications with a 9 μm intrinsic resolution on 2 strip clusters.

The raw silicon detector performance is promising for physics in Run II. With the silicon being used not only in off-line tracking but also in the Level 2 trigger (approximately every 50 μs), tracking information from the COT and silicon are being used to trigger on events with large impact parameters that are interesting for heavy flavor physics. This innovative trigger, called the Silicon Vertex Tracker (SVT), allows CDF to trigger on lepton-less B decays, relieving the penalty of small B leptonic branching fractions and enhancing the fraction of fully reconstructed B decays in the data. Results from CDF Run II are currently being published. Two examples of analyses that rely on the CDF silicon detector are the measurement of the B lifetime from $B \to J/\Psi X$ and the fully hadronic decay $B^{\pm} \to K^{\pm}\phi$ (shown in Figure 1). CDF is now collecting high quality data that is being used in many interesting physics applications.

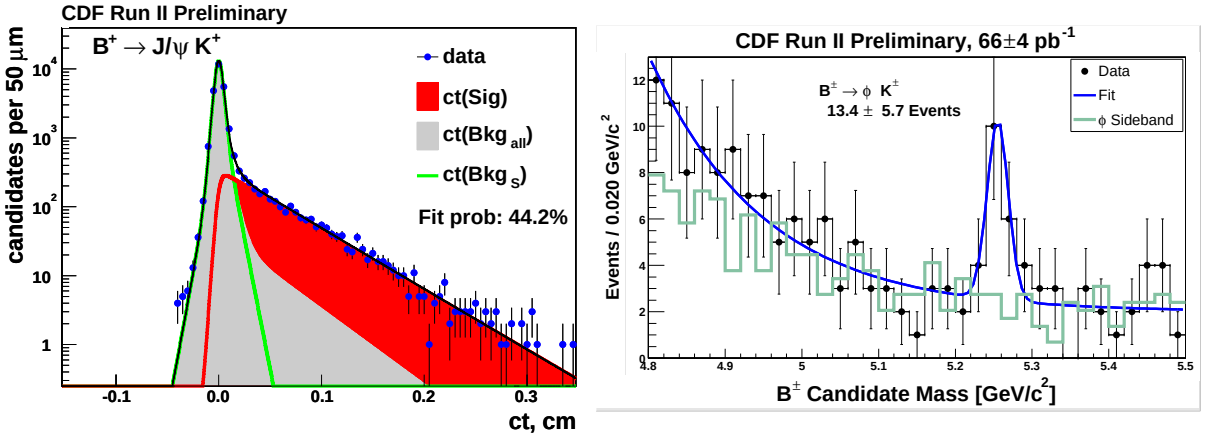

Figure 1: Representative B physics analyses that rely on CDF silicon. The inclusive B lifetime from $B \to J/\Psi X$ is shown on the left and the $B^{\pm}$ mass from $B^{\pm} \to K^{\pm}\phi$ on the right.